
Deliver your EBD model with confidence

EBCConverter V1.0™

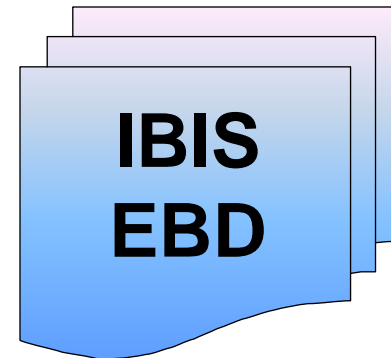
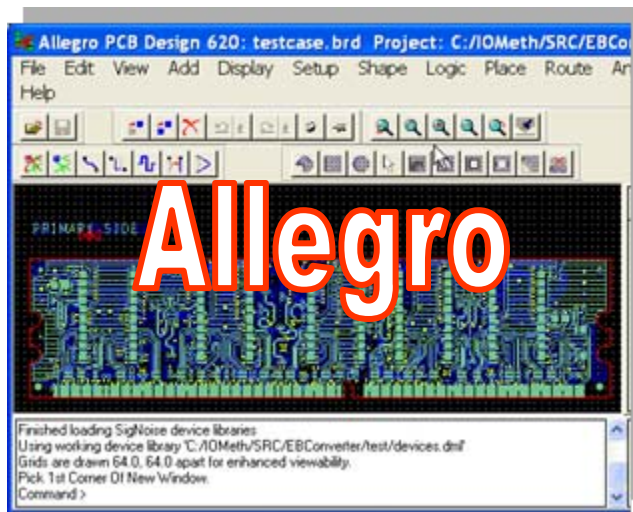
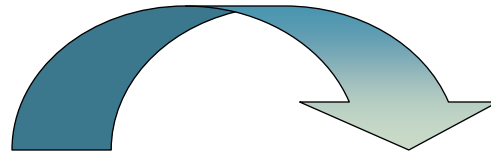
Release 200810

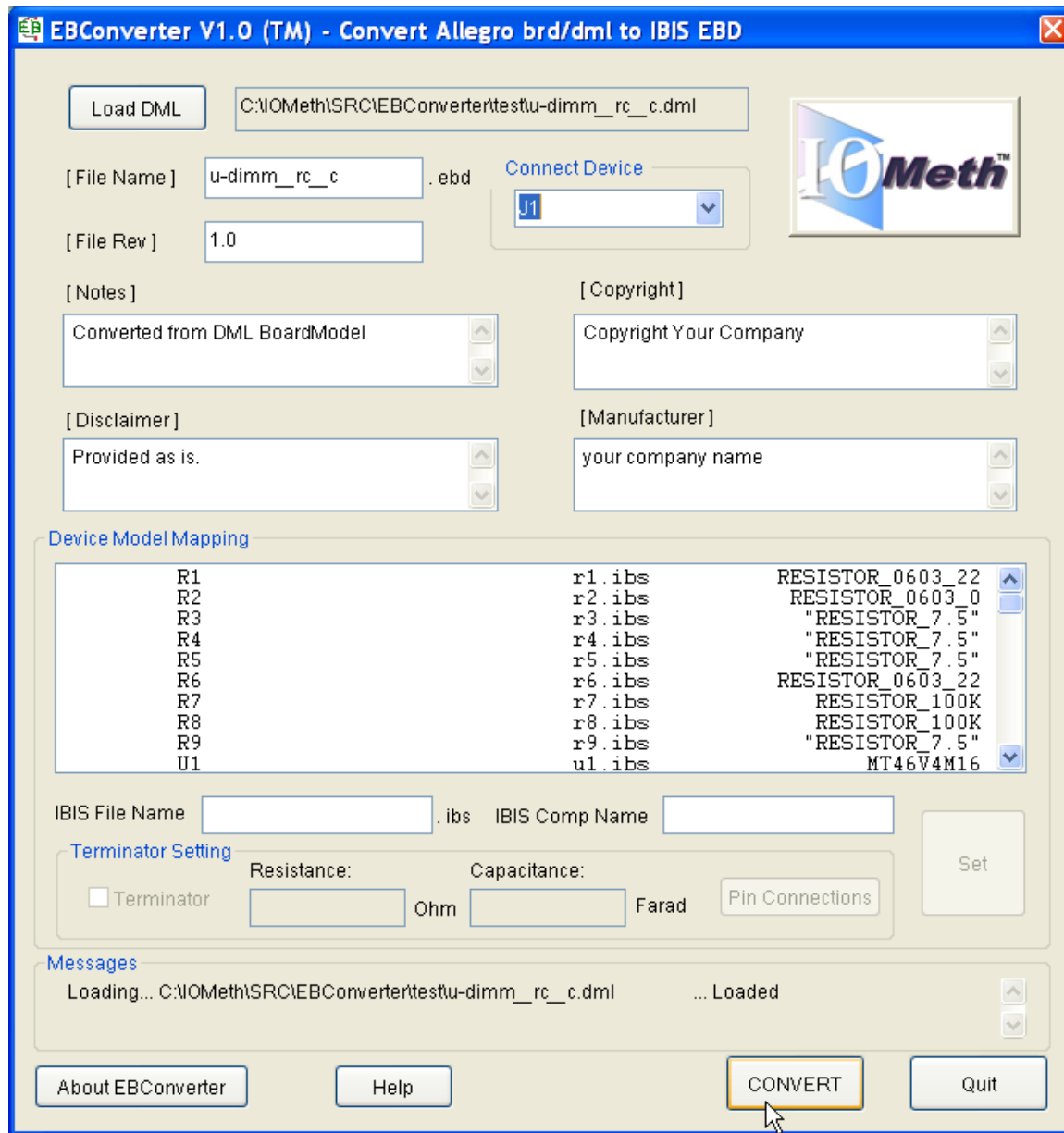
Doc V1.0



EBConverter V1.0™

- Convert your Allegro brd / dmi to IBIS EBD model

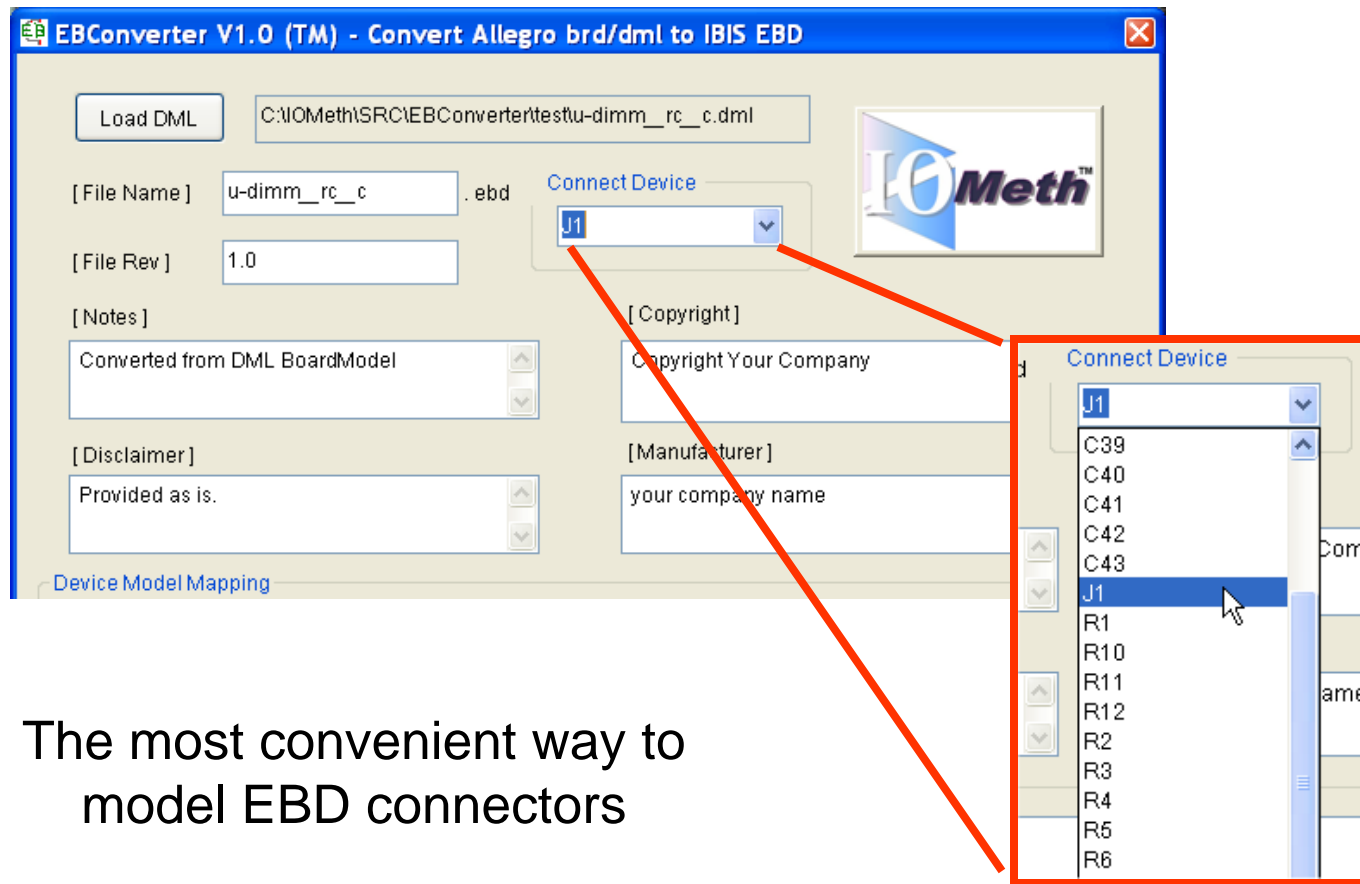




EBConverter V1.0™

- The most accurate IBIS EBD converter on the Market
 - Flexible Connect Device (Connector) selection
 - Complete Connector Pin list
 - Automatic serial/parallel terminator handling for complete extended netlist
 - Automatic embedded terminations in [Path Description] and IBIS Terminator model generations
 - Keep all the data name (Net, RefDes, etc.) as the same as original board
 - Remain DML boardmodel segment names as comment for easy verification

Flexible Connect Device (Connector) Selection



The most convenient way to model EBD connectors

Complete Connector Pin list

```
[Number Of Pins] 184
```

```
[Pin List] signal_name
```

```
| J1.1  
1 POWER  
| J1.2  
2 DQ0  
| J1.3  
3 GND  
| J1.4  
4 DQ1  
| J1.5  
5 DQSO  
| J1.6  
6 DQ2  
| J1.7  
7 POWER  
| J1.8  
8 DQ3  
| J1.9  
9 NC  
| J1.10  
10 NC  
| J1.11  
11 GND  
| J1.12  
12 DQ8  
| J1.13  
13 DQ9  
| J1.14  
14 DQS1  
| J1.15  
15 POWER
```

```
| J1.173  
173 NC  
| J1.174  
174 DQ60  
| J1.175  
175 DQ61  
| J1.176  
176 GND  
| J1.177  
177 DM7  
| J1.178  
178 DQ62  
| J1.179  
179 DQ63  
| J1.180  
180 POWER  
| J1.181  
181 SA0  
| J1.182  
182 SA1  
| J1.183  
183 SA2  
| J1.184  
184 VDDSPD
```

Produced by another tool

```
[Number Of Pins] 172  
[Pin List] signal_name  
1 POWER  
2 DQ0  
3 GND  
4 DQ1  
5 DQSO  
6 DQ2  
7 POWER  
8 DQ3  
11 GND  
12 DQ8  
13 DQ9  
14 DQS1  
15 POWER  
16 CK1  
17 CK1#  
18 GND  
19 DQ10  
20 DQ11  
21 CKEO  
22 POWER  
23 DQ16  
24 DQ17  
25 DQS2
```

**Wrong Pin Mapping
with missing pins !!!**

Robust Terminator Handling

```
[Path Description] DQ0
| J1.2
Pin 2
| R@@X2130Yn370L1_@@J1.2
| ignored for
| Len=0 L=0.000
| XNTL_XSTLX23
| Len=0.00382234
| R@@X2350Y970L1_@@U1.1
| ignored for Spice simulator
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/
| RN1.1 -> RN1.8 R=22
| Len=0 R=22/
| Net: DQ0A
| R@@X2350Y1370L1_@@RN1.8
| ignored for Spice simulators
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/
| XNTL_XSTLX2350Y1370L1X4040Y5321L1
| Len=0.0145933 L=3.6466e-007 C=8.8655e-011 R=4.5129e+000/
| R@@X4040Y5321L1_@@U1.54
| ignored for Spice simulators
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/
Node U1.54
```

**Embedded termination
for extended netlist**

```
[Component] 2PIN_2GR100K
[Manufacturer] Created by EBConverter

[Package]
|-----|
| [Comp] R_pkg typ min max
| [Manu] L_pkg 0 NA NA
| C_pkg 0 NA NA
| [Pack]
| [Pin] signal_name model_name
| R_pkg 1 signal NC
| L_pkg 2 signal term_p0_g0_rp_rg0
| C_pkg [Series Pin Mapping] pin_2 model_name
| 1 2 series_r100K_c

[Pin]
1 signal NC
2 signal term_p0_g0_rp_rg0
[Series Pin Mapping] pin_2 model_name
1 2 series_r0_c
```

**Auto-generation for
IBIS Terminator / Series
models**

```
[Model] term_p0_g0_rp_rg0
Model_type Terminator
| variable typ min max
| C_comp 0 NA NA
| [Pullup Reference] 0 NA NA
| [Pulldown Reference] 0 NA NA
| [POWER Clamp Reference] 0 NA NA
| [GND Clamp Reference] 0 NA NA
|-----|
| [Rgnd] 0 NA NA

[Model] series_r100K_c
Model_type Series
| variable typ min max
| C_comp 0 NA NA
| [Pullup Reference] 0 NA NA
| [Pulldown Reference] 0 NA NA
| [POWER Clamp Reference] 0 NA NA
| [GND Clamp Reference] 0 NA NA
|-----|
| [R Series] 100K NA NA
```

Easy Terminator Work Wizard

- Detect Net connections
- Handles Isolated and Bussed type resistor packs
- Automatic embedding solutions for extended nets

Package Pin Connection (4 Pin)

Name: 4PIN_ISOLATED_

| Net < > RefDes . Pin Name | Pair Pin |
|---------------------------|----------|
| DQ7 < > RN3 . 1 | 4 |
| DQ3 < > RN3 . 2 | 3 |
| DQ3A < > RN3 . 3 | 2 |
| DQ7A < > RN3 . 4 | 1 |

Bussed

Apply Cancel

Terminator Setting

Terminator

Resistance: 22 Ohm

Capacitance: Farad

Pin Connections

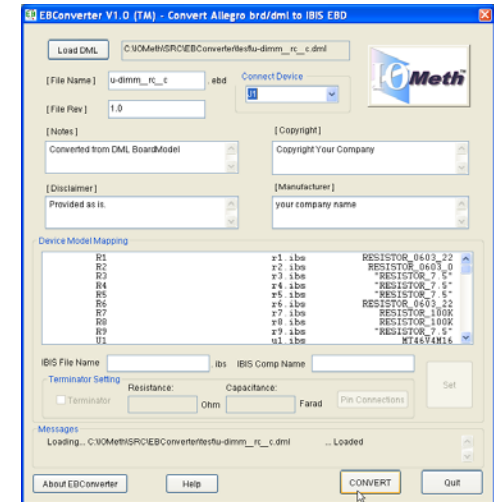
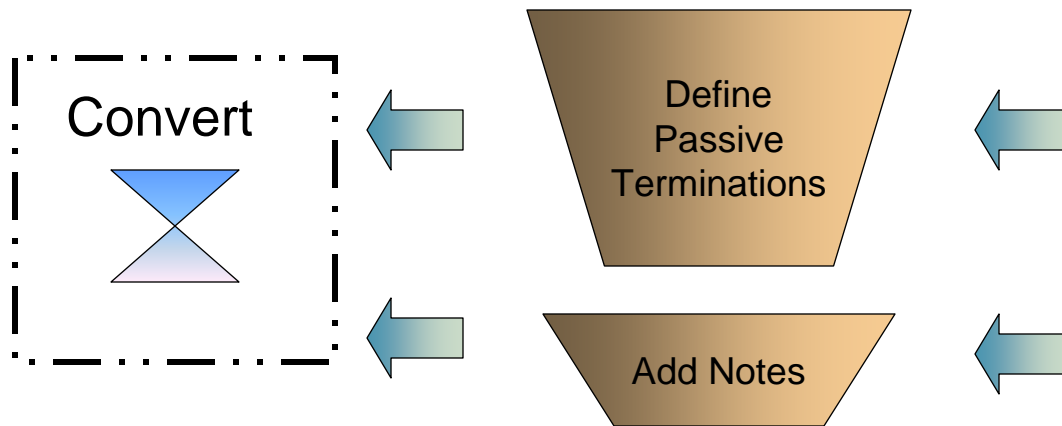
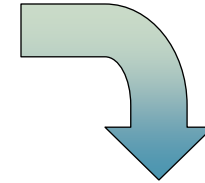
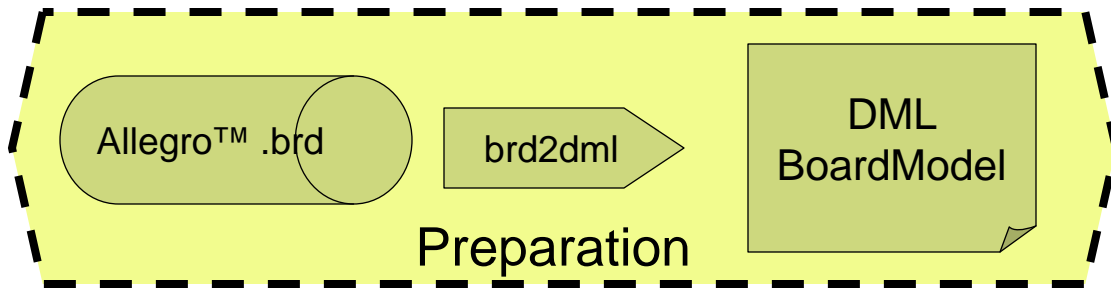
Informational comments/notes

```
|  
[Number Of Pins] 184  
|  
[Pin List] signal_name  
| J1.1  
1 POWER  
| J1.2  
2 DQ0  
| J1.3  
3 GND  
| J1.4  
4 DQ1  
| J1.5  
5 DQSO  
| J1.6  
6 DQ2  
| J1.7  
7 POWER  
| J1.8
```

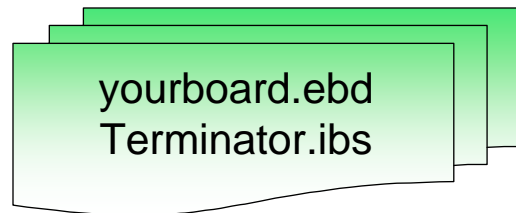
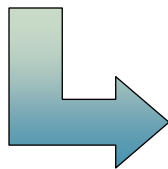
```
[Path Description] DQ0  
| J1.2  
Pin 2  
| R@@X2130Yn370L1_@@J1.2  
| ignored for Spice simulators  
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/  
| XNTL_XSTLX2350Y970L1X2130Yn370L1  
Len=0.00382234 L=3.6466e-007 C=8.8655e-011 R=4.5129e+000/  
| R@@X2350Y970L1_@@RN1.1  
| ignored for Spice simulators  
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/  
| RN1.1 -> RN1.8 R=22  
Len=0 R=22/  
| Net: DQ0A  
| R@@X2350Y1370L1_@@RN1.8  
| ignored for Spice simulators  
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/  
| XNTL_XSTLX2350Y1370L1X4040Y5321L1  
Len=0.0145933 L=3.6466e-007 C=8.8655e-011 R=4.5129e+000/  
| R@@X4040Y5321L1_@@U1.54  
| ignored for Spice simulators  
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/  
Node U1.54
```

**Keep the information as the original board
Remain the segment info in EBD for easy verification**

Process Flow



Load in EBC



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- Convert your Allegro brd / dml to IBIS EBD model

Do Quick!

Done Right!