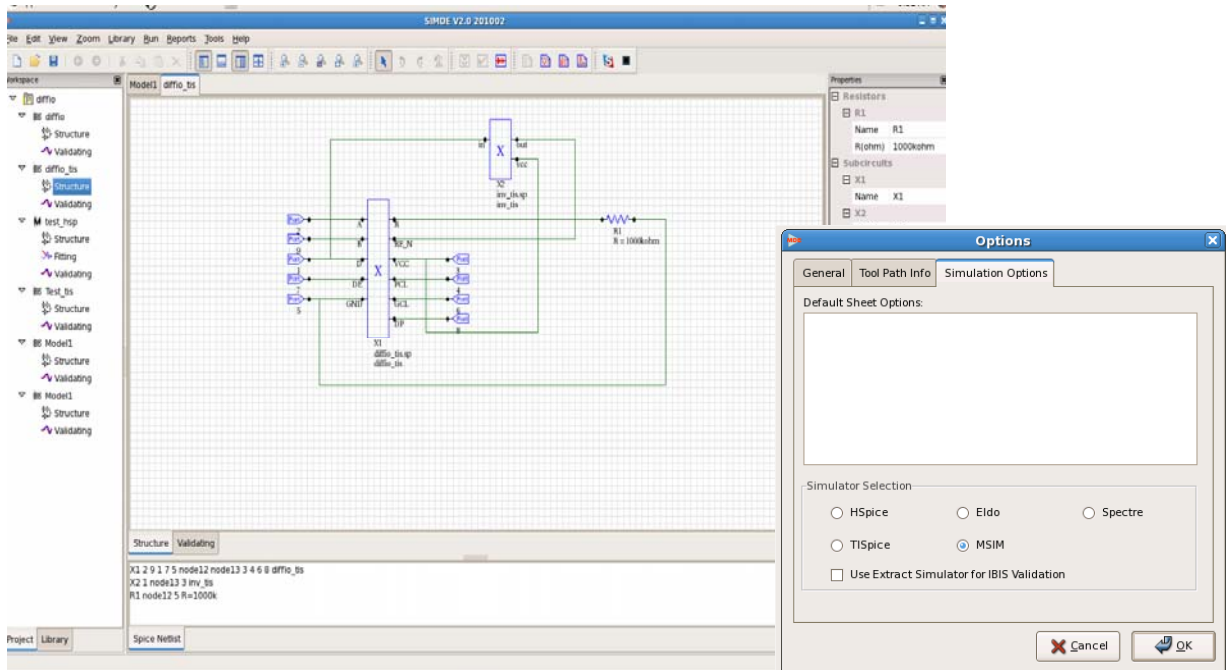


# SIMDE™ V2.2

The environment for Signal Integrity model generation and validation



## SIMDE™ Overview

- Automated IBIS Model Generation for
  - All types of IBIS buffer
  - True differential pair buffer using traditional IBIS buffers
- Automated SPICE macromodel generation with embedded Fitting functionality
  - Pre-emphasis
  - SSO/SSN driver and receiver
  - Analog models

Simulation is more and more important for High-Speed system design. It can help you optimize your design performance, reduce your design cycle, lower your prototype cost and accelerate your design to market. Electrical I/O modeling is the starting point for your advanced chip and system simulations. It enables faster and more accurate simulations.

Signal Integrity Model Development Environment (SIMDE™) provides a graphical model development and validation environment. It gives direct methods for model development and validation. It focuses on automated SI model generation and validation processes (IBIS and SPICE macromodeling in this version and Verilog-A / VHDL-AMS in the future).

Create accurate models, more quickly.

## IBIS Model Generation and Validation

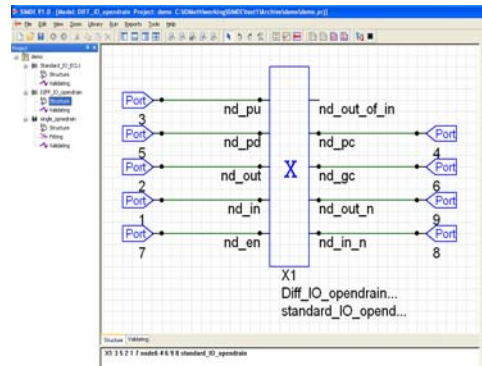
SIMDE™ provides an automated IBIS buffer model generation and validation process. It includes a graphical interface for mapping the SPICE buffer nodes as well as using the schematic type editing mode for other nodes settings. It automatically runs Synopsys HSpice to extract the buffer's behavior from the Spice buffer. There is no need for manual editing during the process.

SIMDE™ has a seamless validation process for IBIS buffer model generation. It remembers all the settings for the Spice model when generating the IBIS buffer and uses them for your IBIS model validation on your own topologies. It also provides a detailed DPI (Differential Peak Index) and DAI (Differential Average Index) and reports any differences between the Spice and IBIS buffer simulations. A waveform clearly depicts the quality of the results.

SIMDE™ contains:

- Automatic Spice buffer node mapping capability
- Graphical node setting capability
- Automatic Spice to IBIS buffer extraction process
- Auto Die-Capacitance extraction option for both driving and receiving mode.
- Capable for All IBIS Input / Output / IO model types and differential buffers (Pseudo, half and true differential pair) extractions with manual common-mode voltage setting option
- Easy setup for Typical / Minimum / Maximum corner extractions
- Supports HSpice, Spectre, Eldo, MSIM and TISpice3 integrations \*
- Extraction using existing data for IBIS and IBIS differential models
- Build-in IBIS standard buffer test fixtures
- IBIS buffer model validation sheet with freedom of topology settings

- Detail validation reports with Differential Peak Index (DPI) and Differential Average Index (DAI)
- IBIS buffer curves visual inspection and report for On-die termination, non-monotonic and load-line crossing verification. (SignalMeth™ IBIS Application Module)
- IBIS file generation wizard with [Model Selector] builder



## Spice Macromodel Generation, Fitting and Validation

SIMDE™ also provides an integrated flow for Spice Macromodel Generation, Fitting and Validation. It allows a user to start from scratch or start from the base elements, using our integrated standard library elements or elements you made as black-boxes. Its hierarchy structure will give the user a clean graphical structural view from the different levels.

The Fitting process allows the user to load the Golden waveform for the macromodel optimization process. It can swing many parameters and find the best settings for the case that fits the Golden source the best.

The validation process takes place in an easy-to-use environment for verifying the macromodel that you just built for a specific load validation. You may also import 3<sup>rd</sup> party models for validation.

The Spice macromodel is powerful and fast. It can virtually model everything you may need.

### Product Configurations (Available for Windows and Linux OS platforms)

Features		Tiers	IBIS	IBISDIFF	MACROMODEL
IBIS Generation (Single-end)	I/O		X	X	
	Input		X	X	
	Output		X	X	
	Open_drain		X	X	
	Open_source		X	X	
	Open_sink		X	X	
	ECL		X	X	
Terminator		X	X		
IBIS Validation (Single-end)	I/O		X	X	X
	Input		X	X	X
	Output		X	X	X
	Open_drain		X	X	X
	Open_source		X	X	X
	Open_sink		X	X	X
	ECL		X	X	X
Terminator		X	X	X	
IBIS Generation (differential)	I/O			X	
	Input			X	
	Output			X	
	Open_drain			X	
	Open_source			X	
	Open_sink			X	
	ECL			X	
Terminator			X		
IBIS Validation (differential)	I/O			X	X
	Input			X	X
	Output			X	X
	Open_drain			X	X
	Open_source			X	X
	Open_sink			X	X
	ECL			X	X
Terminator			X	X	
Topology Editor	Parameter Fitting				X
	Continuously Parameter sweep				X
	Typ/min/max parameter sweep		X	X	
	Build-in test circuit		X	X	
	Free form circuit				X
Simulator	Multi-simulator support		X	X	X
	Build-in IBIS validation simulator		X	X	X

### Product Support / Maintenance

This is a yearly fee-based service including technical Q&A, bug fixing service packs and product enhancement updates. Product technical training is available for an additional cost to customers on maintenance.

\* Spectre, TiSpice3 integrations are only available for Linux OS.