
SimDETM *MODEL*

Modeling your device with performance and accuracy

V3.1 - Release 201109



What's New in V3.1 201109

- SimDE™ MODEL supports IBIS 5.0 PDN features for all simulators with build-in PDN test circuits
- More extraction accuracy improvements
- SimDE™ IBIS VALIDATOR available for IBIS model viewing, checking and validations
- SimDE™ WAVEFORM supports 3D data views
- SimDE™ WAVEFORM supports all IBIS 5.0 PDN curve viewing capability

SimDE™ MODEL

- **The first complete IBIS model development and validation tool**
 - Support all IBIS buffer type extraction / generation
 - Automated differential IBIS model (True, Pseudo and Half) extraction / generation
 - Integrated IBIS model validation for single-end and differential-pair IBIS buffers
 - Support IBIS 5.0 PDN feature extractions
- **The industry first Spice Macromodel development tool with Fitting and Validating functionalities**
 - Support advance digital buffer model development
 - Automated Fitting and Validating functionalities with golden waveforms
 - Support analog model development

IBIS 5.0 PDN features with build-in test circuit

The screenshot displays the SimDE MODEL V3.1 201109 interface. The main window shows a circuit diagram with components including V2 (DC = 3.3V), V1, VCP1, VCP2, RLC1, RLC2, U1, and T1. The circuit is connected to a stimulus source and includes probes (probe1, probe2). The Buffer Model Creation Preference dialog box is open, showing various simulation settings. The 'Use DC Analysis Mode' checkbox is circled in red.

Buffer Model Creation Preference

Warning / Correction Threshold Setting

| | Warning | Correction |
|----------------------------------|---------|------------|
| Clamp Terminator (MegaOhm): | 5000 | 3000 |
| VT/IV Curve Match Tolerance (%): | 1 | 5 |

C_comp Setting

Frequency For C_comp Extraction (MHz): 200

Spice V-T Curve Simulation Setting

Static Delay (ns): 0

Pulse Delay: UI(ns): 1 Cycles: 0

Stimulus Levels

| | Typical | Minimum | Maximum |
|----------|---------|---------|---------|
| High (V) | 3.3 | 3.1 | 3.5 |
| Low (V) | 0 | 0 | 0 |

Spice I-V Curve Simulation Setting

Transient Analysis

Step (ns): 20 Delay (ns): 20

Step - the measurement time step size for capturing the current
Delay - the time delay before measurement starts

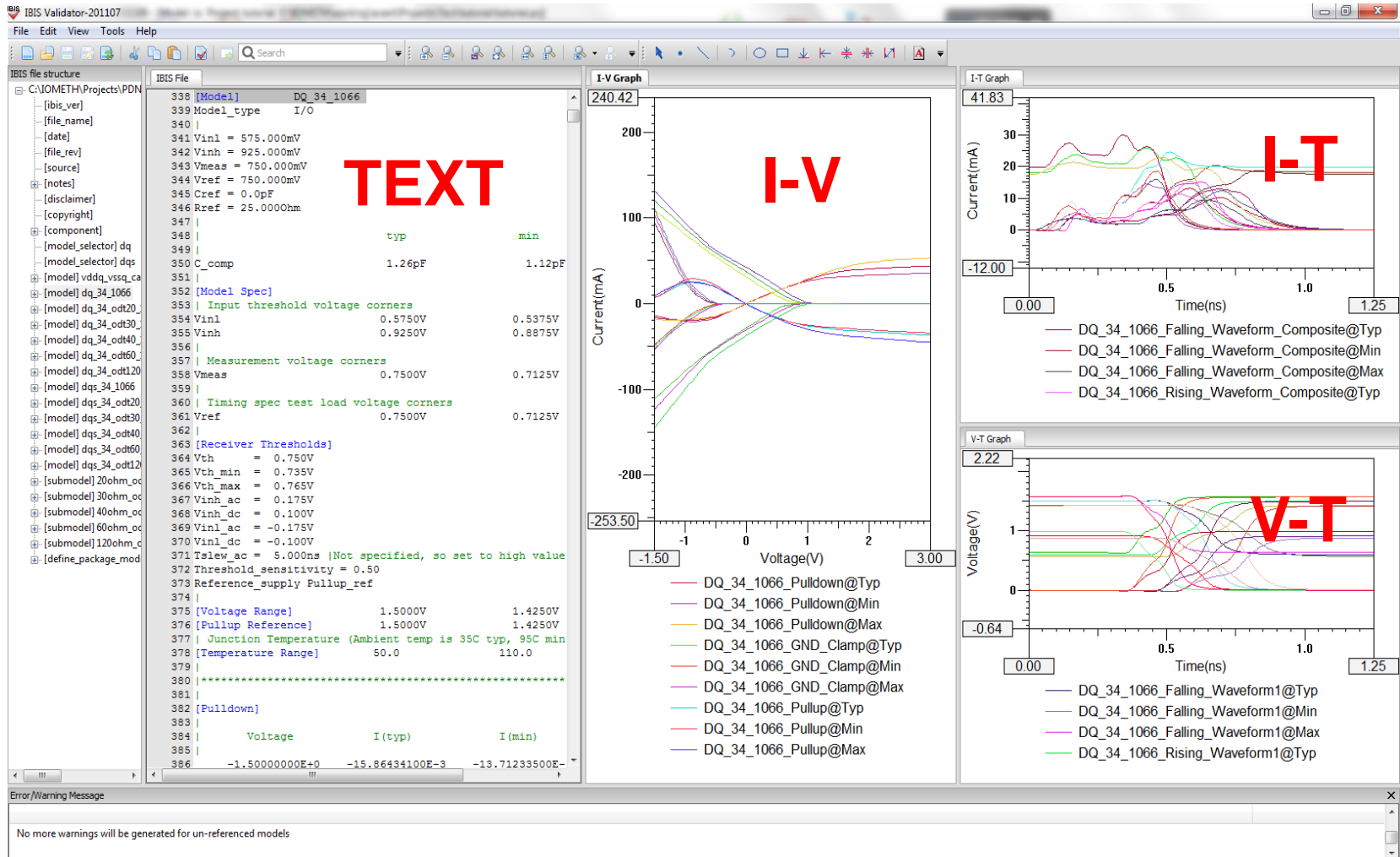
Use DC Analysis Mode

PDN Features

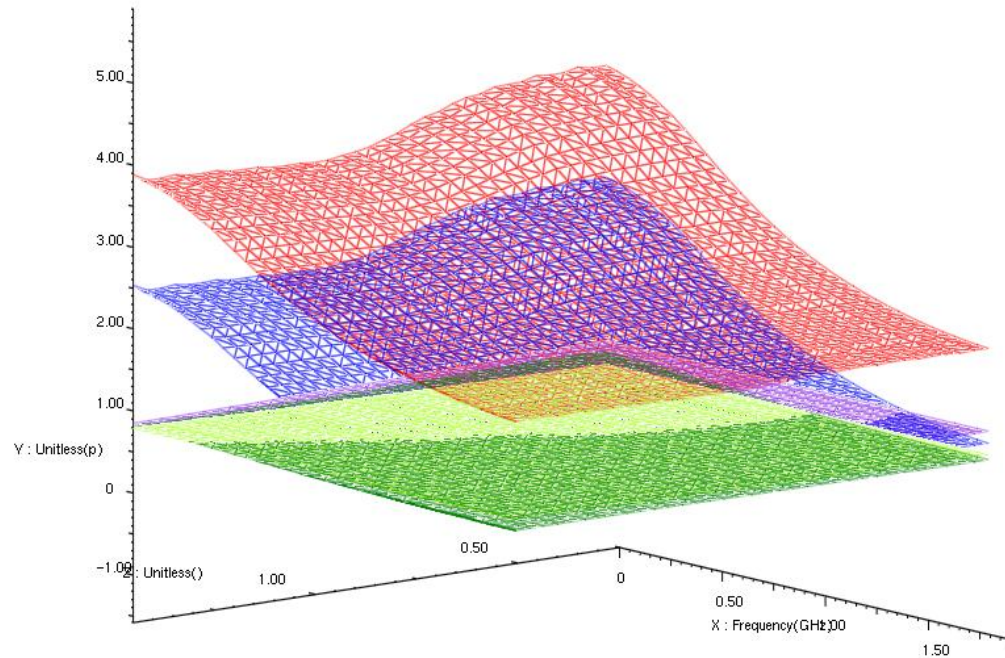
Composite Current ISSO

OK Cancel

IBIS VALIDATOR



WAVFORM 3D View



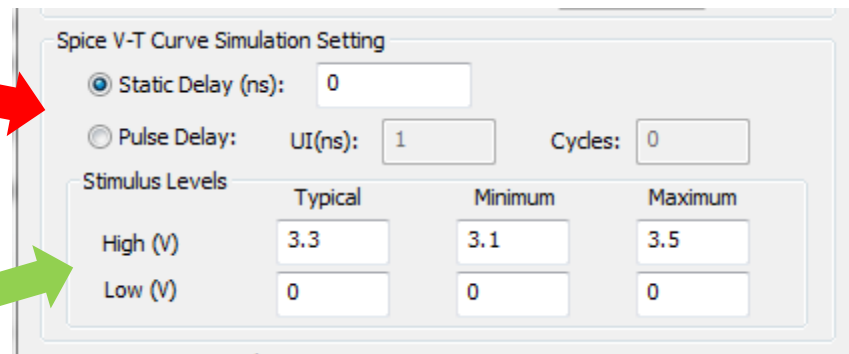
Flexible stimulus controls for IBIS model generations

■ Delays

- Static
- Pulse

■ Levels

- High/Low
- Typ/Min/Max



Spice V-T Curve Simulation Setting

Static Delay (ns): 0

Pulse Delay: UI(ns): 1 Cycles: 0

| Stimulus Levels | Typical | Minimum | Maximum |
|-----------------|---------|---------|---------|
| High (V) | 3.3 | 3.1 | 3.5 |
| Low (V) | 0 | 0 | 0 |

Stimulus level control for different corner IBIS validations

The screenshot displays a circuit simulation environment with a grid background. A voltage source labeled 'V1' is connected to a signal line labeled 'stimulus'. A probe labeled 'probe1' is connected to the signal line. Two dialog boxes are open: 'Stimulus Generator' and 'Parameter editor'.

The 'Stimulus Generator' dialog box has the following settings:

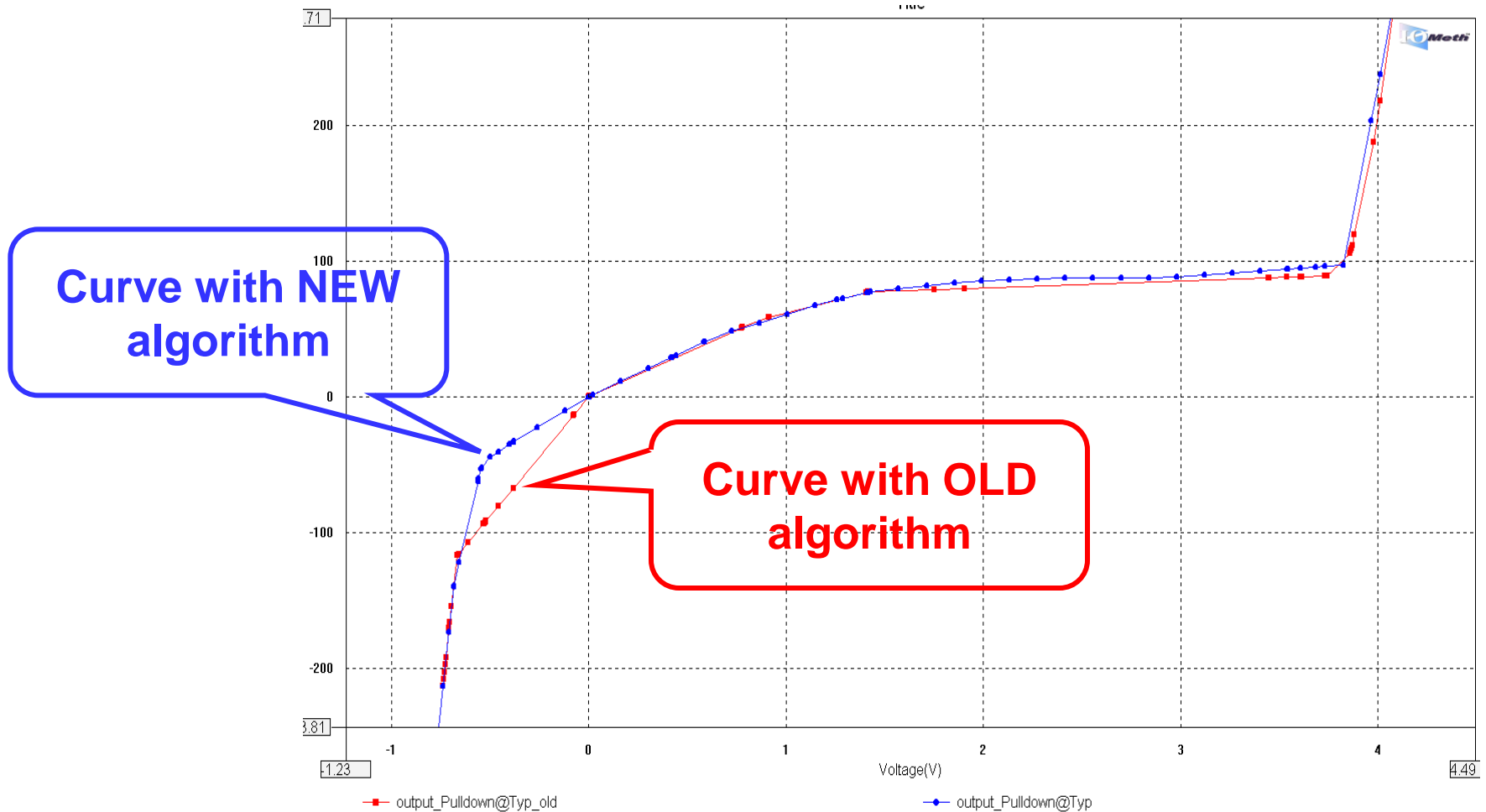
- PRBS4 (selected)
- Differential (unchecked)
- Unit Interval: 25ns
- High Level: \$shigh (circled in red)
- Jitter: 0s
- Customized Bits: (empty)

The 'Parameter editor' dialog box shows a table with the following data:

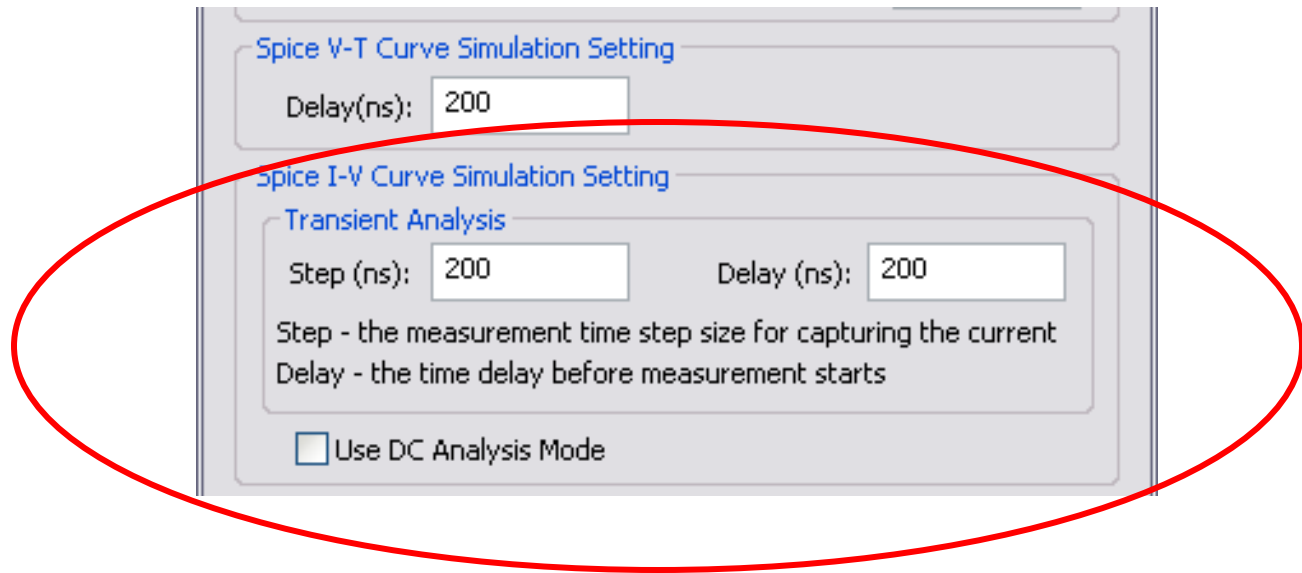
| Name | Typical | Slow | Fast |
|---------|---------|------|------|
| \$shigh | 3.3 | 3.1 | 3.5 |

A red arrow points from the 'High Level' field in the 'Stimulus Generator' dialog box to the '\$shigh' row in the 'Parameter editor' dialog box.

Advanced “weighted” Best-Point algorithm for I-V curve representations



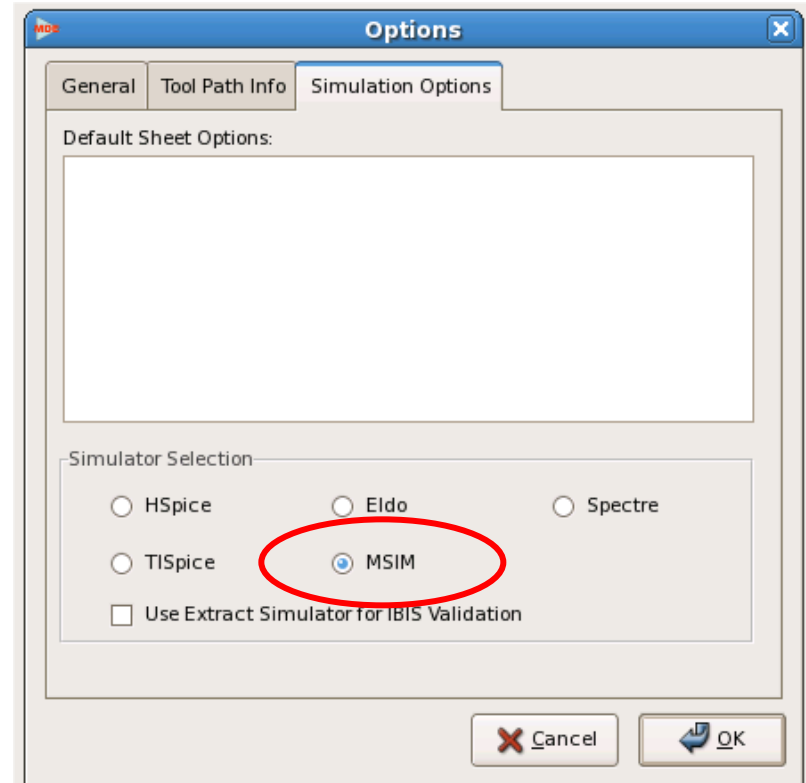
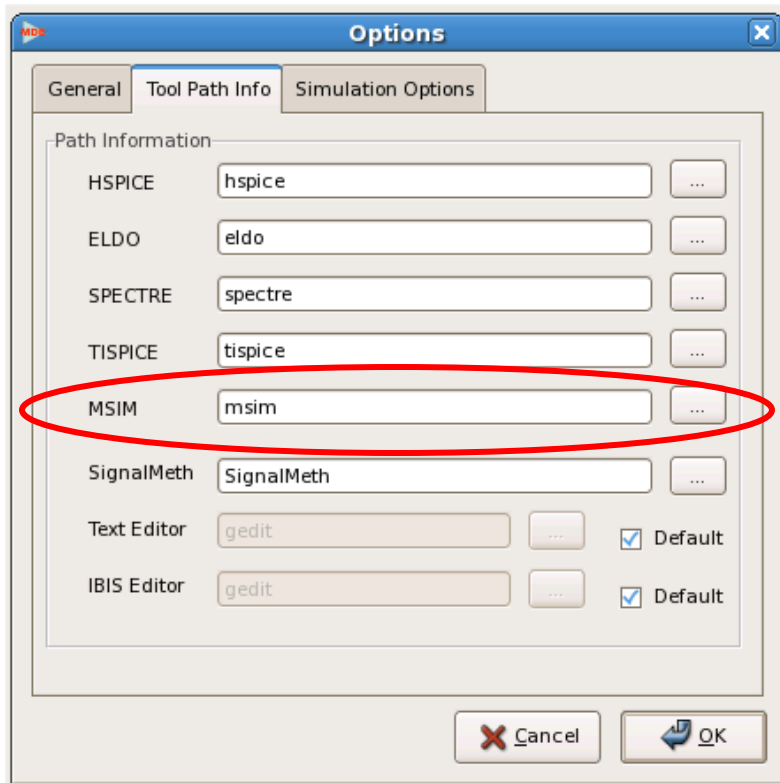
Both Transient and DC analysis modes available for I-V curve extractions



Insured to get the best result for I-V curve extractions

Spectre DC Analysis mode is not available in V2.2

Integrated MSIM simulator support for extraction and validation



Model Selector Builder

- Build [Model Selector] from different IBIS files
- Load, Edit, Remove functionalities
- Can be added as a pin in IBIS file generation wizard

in_p out_n

in_r out_p

Port 9

Port 3

Port 5

IBIS Model Selector Builder

[Model Selector] DQ

| Model Name | Descriptions |
|------------|--------------|
| DQ_FULL | DQ_FULL |
| DQ_HALF | DQ_HALF |

Load Edit Remove

Available Models

| Model Name | Model Type |
|------------|------------|
| DQ_FULL | 3-state |
| DQ_HALF | I/O |

Add

Location: []

IBIS File: C:\[OMeth\working\avant\Projects\Test\tutorial\IBIS_Files\[] Browse

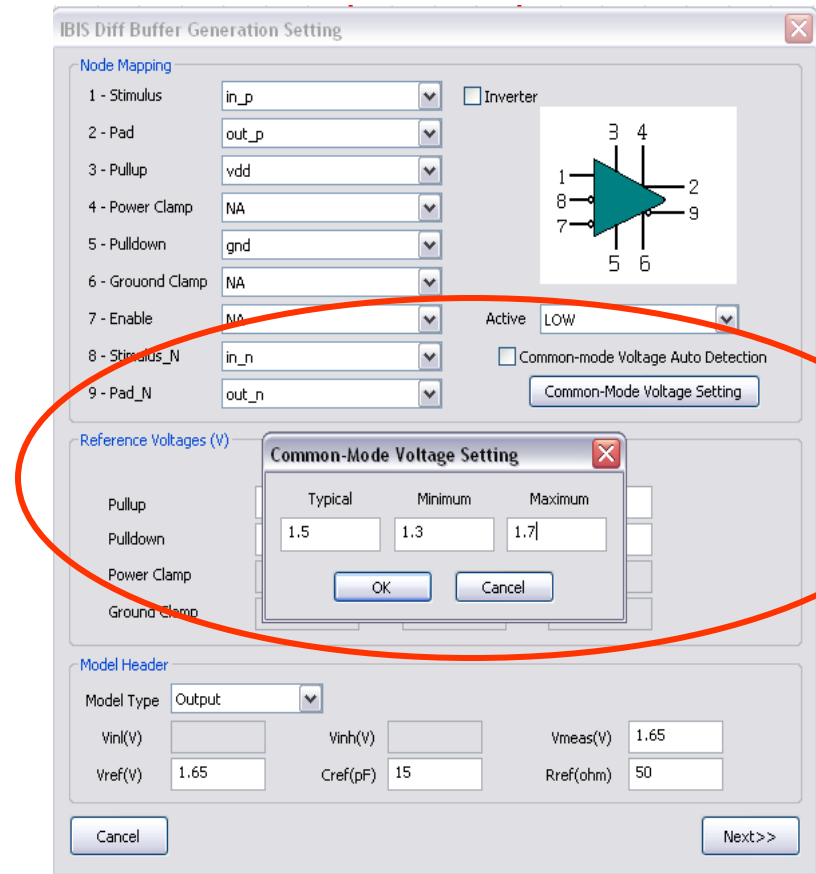
Model Type: All Buffers

Build Cancel

| pin | R_pin | L_pin | C_pin |
|-----|-------|--------|---------|
| | 81m | 6.00nH | 0.903pF |
| | 128m | 5.44nH | 0.980pF |
| | 127m | 5.33nH | 0.957pF |
| | 110m | 4.76nH | 0.801pF |
| | 107m | 4.81nH | 0.687pF |

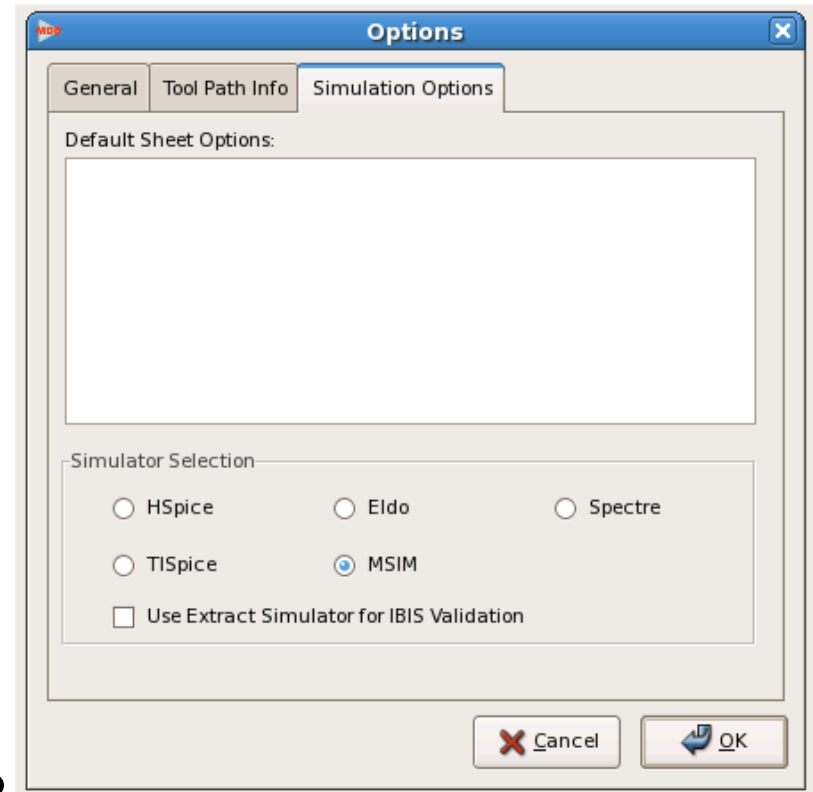
Manual Common-mode voltage setting option for differential pair IBIS extractions

- Manual common-mode voltage setting option
- Auto-detection still available
- Increase IBIS buffer model accuracy by setting precision common-mode voltages for each corner



Multiple Simulator integrations

- Supports
 - Synopsys HSpice
 - Cadence Spectre
 - Mentor Eldo
 - Texas Instrument Spice3
 - Legend MSIM
- Seamless switching capability



IBIS Buffer Generation

The screenshot displays the SIMDE V1.0 interface for an IBIS buffer model. The main schematic shows a central component 'X1 sIO_33.sch sIO' with various pins connected to a circuit. A voltage source 'V2 DC = 1V' is connected to the 'deq' pins. A parameter 'V1 DC = \$vddval' is connected to the 'vddaux' pin. The schematic also shows connections to 'vdd' and 'vss' through ports.

A 'Parameter editor' window is open, showing the following table:

| Name | Typical | Slow | Fast |
|----------|---------|------|------|
| \$vddval | 1 | 0.75 | 1.25 |

Yellow callout boxes highlight key features:

- Graphical Settings:** Points to the schematic components and their connections.
- Conditional Parameters:** Points to the parameter 'V1 DC = \$vddval'.
- Configurable Blackbox:** Points to the central component 'X1 sIO_33.sch sIO'.

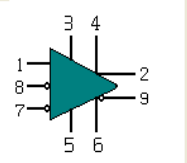
The status bar at the bottom indicates 'Structure Validating' and 'HSpice'.

IBIS Generation Setting Wizards

IBIS Diff Buffer Generation Setting

Node Mapping

1 - Stimulus: dp Inverter
 2 - Pad: bxp
 3 - Pullup: vtt
 4 - Power Clamp: NA
 5 - Pulldown: vss
 6 - Ground Clamp: NA
 7 - Enable: NA Active: LOW
 8 - Stimulus_N: dn
 9 - Pad_N: bxn



Reference Voltages (V)

| | Typical | Minimum | Maximum |
|--------------|---------|---------|---------|
| Pullup | 1.5 | 1.1 | 1.9 |
| Pulldown | 0 | 0 | 0 |
| Power Clamp | 1.5 | 1.1 | 1.9 |
| Ground Clamp | 0 | 0 | 0 |

Model Header

Model Type: Output

Vin(V): Vinh(V): Vmeas(V): 0.75
 Vref(V): 0.75 Cref(pF): 15 Rref(ohm): 50

Cancel Next>>

Node Mapping

C_comp Extraction

IBIS Buffer Parameter Setting

C_Comp (pF)

Extract
 Typical: Minimum: Maximum:

Temperature (Centigrade Degree)

Typical: 25 Minimum: 100 Maximum: 0

Test Fixture

R_fixture(ohm): 50 C_fixture(pF): 0

Spice VT Curve Simulation Setting

.TRAN Setting Time Step (ps): 25 Time Stop (ns): 15

LIB

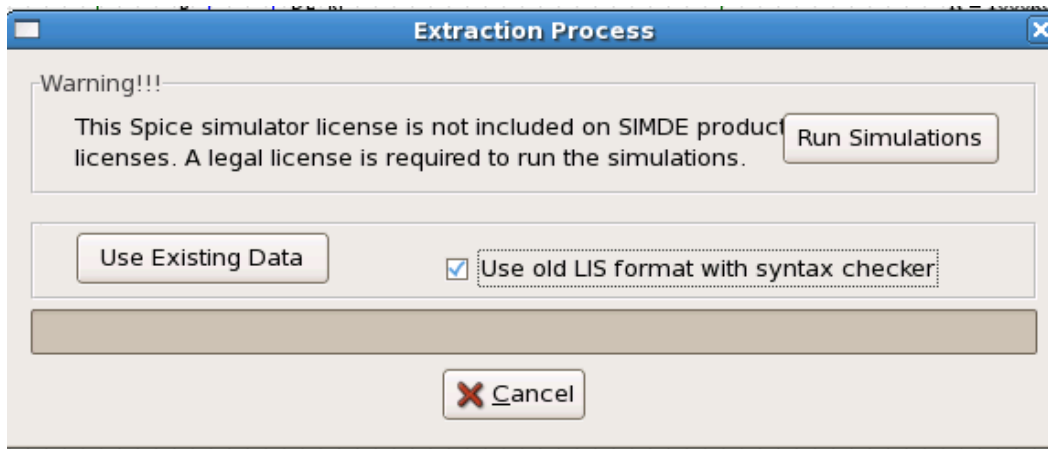
| Lib File | Lib | Typ | Slow | Fast |
|------------------------------|---------|-------------------------------------|--------------------------|--------------------------|
| C:\Meth\working\S... TT_g | TT_g | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| C:\Meth\working\S... tt | tt | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| C:\Meth\working\S... TT_33 | TT_33 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| C:\Meth\working\S... TT_na33 | TT_na33 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| C:\Meth\working\S... DIO | DIO | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| ... | | | | |

Cancel Preference << Previous OK

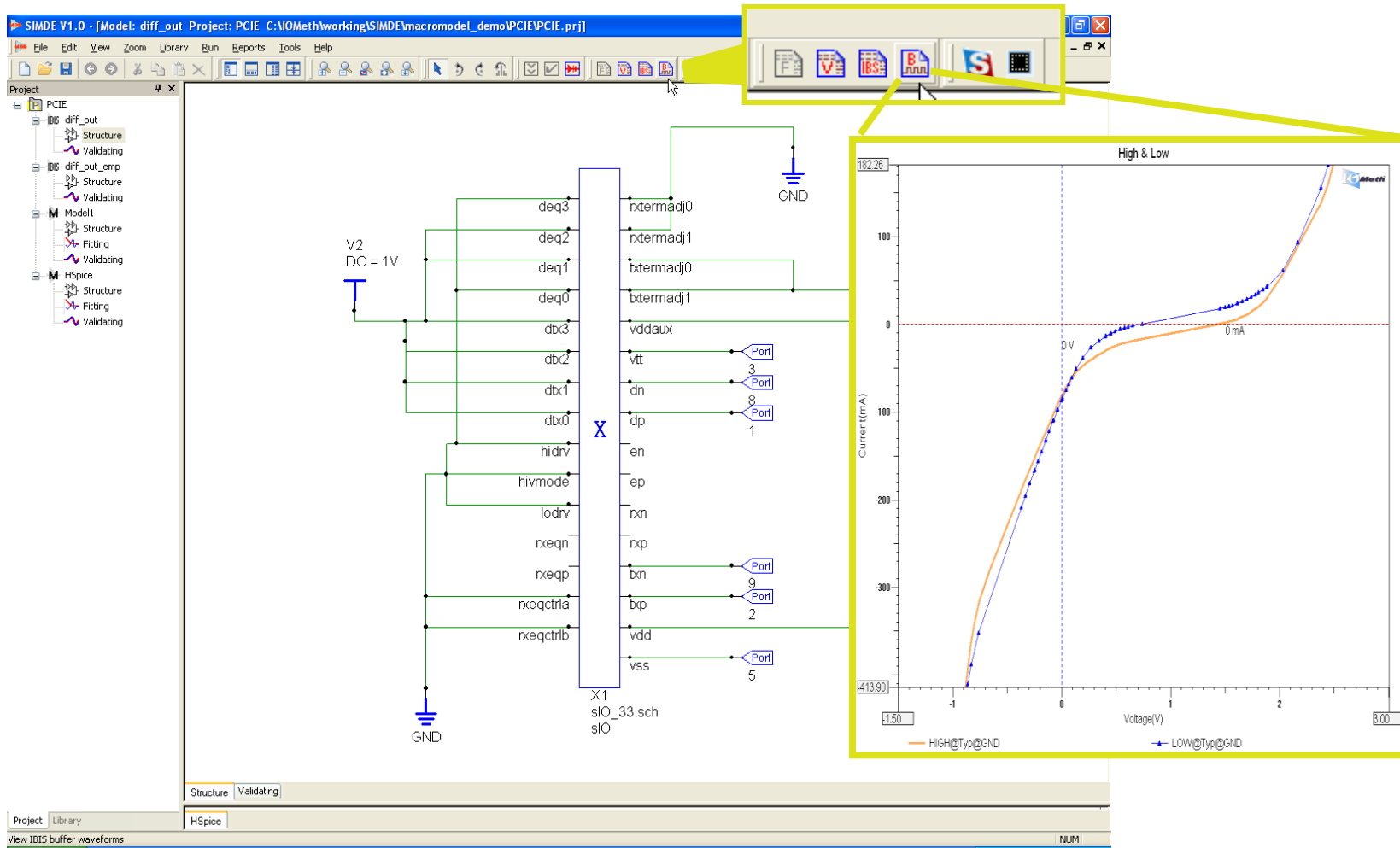
Node Mapping

Extraction with existing data

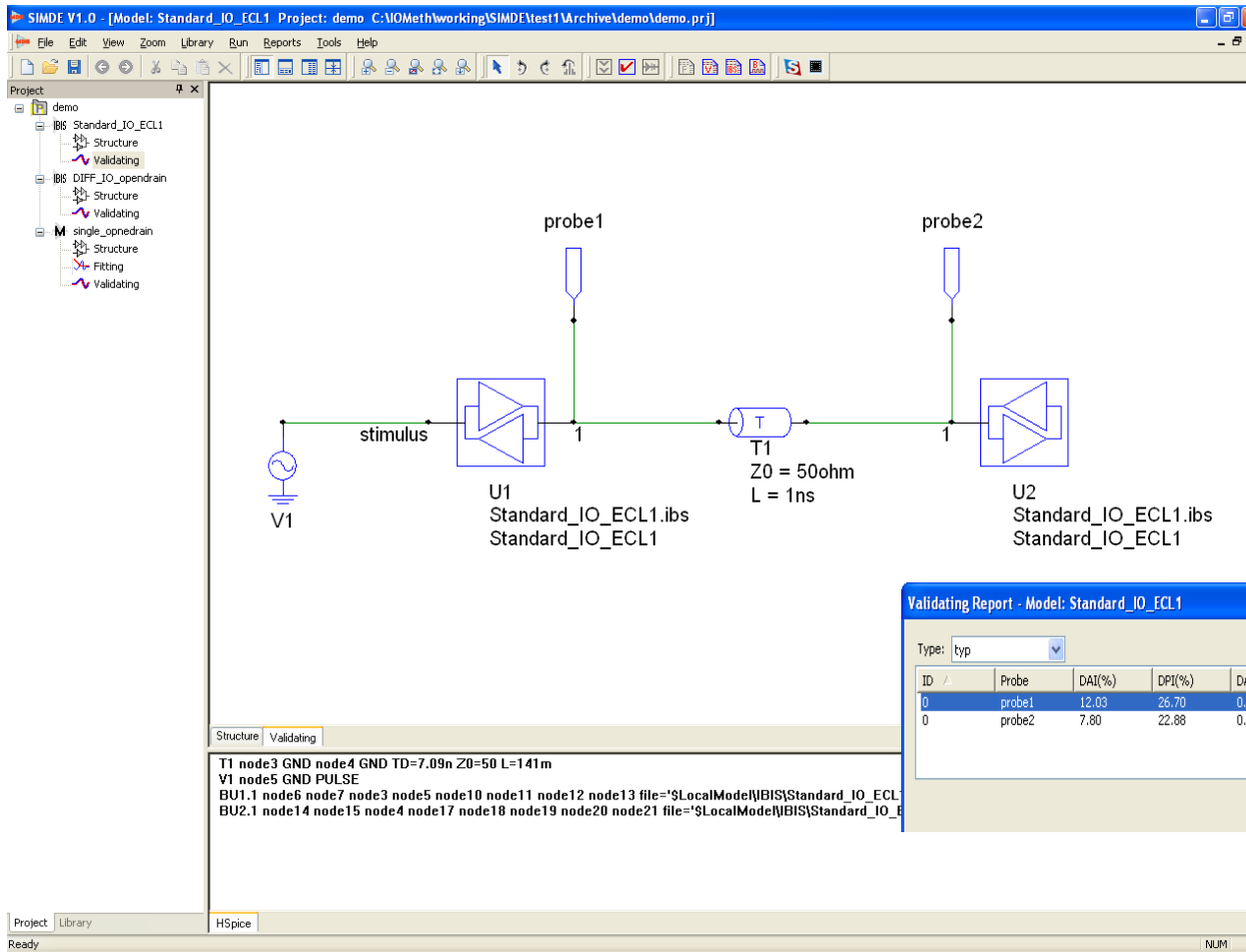
- Save simulation time
- Capable for other simulator and / or measurement output
- With syntax checker



Easy IBIS curve inspection



Build-in Test circuit and Flexible Topology Editor for Validations



Differential report

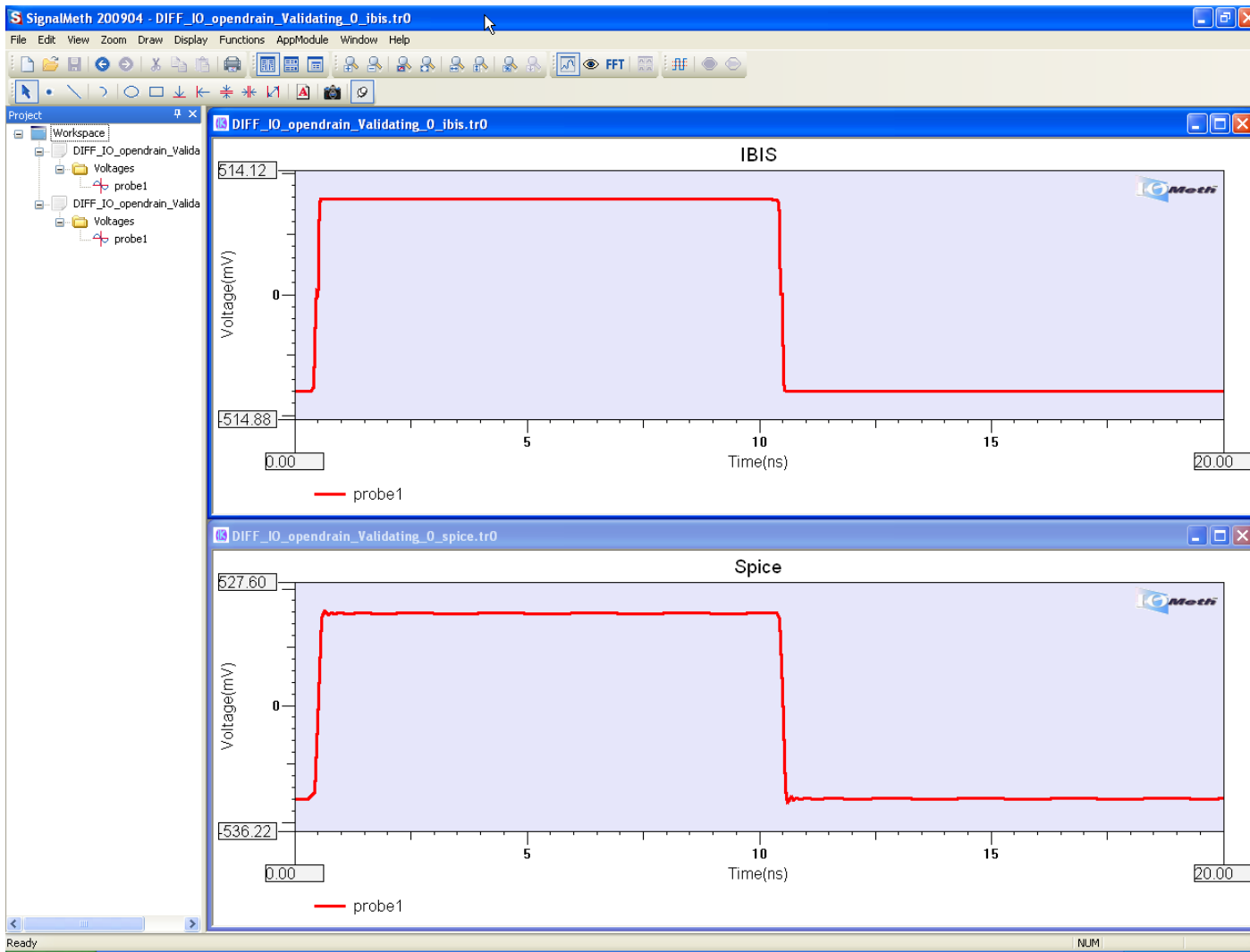
Validating Report - Model: Standard_IO_ECL1

Type: typ

| ID | Probe | DAI(%) | DPJ(%) | DA | DP |
|----|--------|--------|--------|------|------|
| 0 | probe1 | 12.03 | 26.70 | 0.09 | 0.19 |
| 0 | probe2 | 7.80 | 22.88 | 0.09 | 0.28 |

Buttons: IBIS Sim Log, Spice Sim Log, View Waveform, Close

Seamless Validation



Comprehensive IBIS File Builder

Creating IBIS Component

File Name:

[Component]:

[Package]

| Type | Min | Max |
|-------|---------------------------------|---------------------------------|
| R_pkg | <input type="text" value="0m"/> | <input type="text" value="0m"/> |
| L_pkg | <input type="text" value="0n"/> | <input type="text" value="0n"/> |
| C_pkg | <input type="text" value="0p"/> | <input type="text" value="0p"/> |

Diff Pair

| [Pin] | Signal_Name | Model_Name | Model_Type | Diff_pin | R_pin | L_pin | C_pin |
|-------|-------------|------------|------------|----------|---------|-----------|-----------|
| 2 | Q0B | QOUT | Output_ECL | (+)1 | 0.45016 | 2.31200nH | 0.39282pF |
| 1 | Q0 | QOUT | Output_ECL | (-)2 | 0.41551 | 2.46728nH | 0.46661pF |

IBIS Component - Add Pin

[Pin]:

Signal Name:

Signal Model:

Power Ground Signal NC

Pin Parasitics

R_pin: L_pin: C_pin:

Signal Information

Location:

Model File:

IBIS Component:

Model Type:

| [Pin] | Signal_Name | Model_Name | Diff_pin | R_pin | L_pin | C_pin |
|-------|-------------|------------|----------|---------|-----------|-----------|
| 1 | Q0 | QOUT | | 0.41551 | 2.46728nH | 0.46661pF |
| 2 | Q0B | QOUT | | 0.45016 | 2.31200nH | 0.39282pF |
| 3 | Q1 | QOUT | | 0.45022 | 2.31675nH | 0.39342pF |
| 4 | Q1B | QOUT | | 0.41536 | 2.47060nH | 0.46538pF |
| 6 | DB | DIN_S | | 0.24315 | 1.88180nH | 0.44363pF |
| 7 | D | DIN_S | | 0.24302 | 1.86517nH | 0.44245pF |

Macromodel Builder

The screenshot displays the SIMDE V1.0 interface for a PCIe model. The main workspace shows a circuit diagram with the following components and connections:

- Ports:** 'inp' and 'inn' on the left; 'outp' and 'outn' on the right.
- Delay Blocks (X1, X2):** Labeled 'delay_ckt.sp DELAY_CKT'. They receive 'od_din' and 'eq_din' signals and output 'stimulus_P' and 'stimulus_N'.
- Inverters (U1, U2):** Labeled 'test.ibs'. U1 has inputs 'stimulus_P' and 'stimulus_N' and outputs 'diff_out_p' and 'diff_out_n'. U2 has inputs 'stimulus_P' and 'stimulus_N' and outputs 'diff_out_emp_p' and 'diff_out_emp_n'.
- Ground:** A 'GND' symbol is connected to the 'vss' inputs of the delay blocks.

The Properties panel on the right shows the following details:

- Subcircuits:**
 - X1: Name X1, tcy: 1000e-12
 - X2: Name X2, tcy: 1000e-12
- Buffers:**
 - U1.1(+), U1.1(-): Reference Nar U1, Power On, pu_sca=1, pd_sca=1, pc_sca=1, gc_sca=1, c_com_pu=NA, c_com_pd=NA, c_com_pc=NA, c_com_gc=NA, rwf_sca=1, fwf_sca=1
 - U2.3(+), U2.3(-): Reference Nar U2, Power On, pu_sca=1, pd_sca=1, pc_sca=1, gc_sca=1, c_com_pu=NA, c_com_pd=NA, c_com_pc=NA, c_com_gc=NA, rwf_sca=1, fwf_sca=1
- Pins:**
 - inp: Name inp
 - inn: Name inn
 - outp: Name outp
 - outn: Name outn

The console window at the bottom contains the following definitions:

```

BU1.1 node33 node34 outp node37 node38 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs'
model='diff_out_p' Power=On pu_sca=1 pd_sca=1 pc_sca=1 gc_sca=1 rwf_sca=1 fwf_sca=1
BU1.2 node39 node40 outn node43 node44 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs'
model='diff_out_n' Power=On pu_sca=1 pd_sca=1 pc_sca=1 gc_sca=1 rwf_sca=1 fwf_sca=1
BU2.3 node13 node14 outp node31 node17 node18 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs'
model='diff_out_p' Power=On pu_sca=1 pd_sca=1 pc_sca=1 gc_sca=1 rwf_sca=1 fwf_sca=1
BU2.4 node19 node20 outn node29 node23 node24 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs'
model='diff_out_emp_n' Power=On pu_sca=1 pd_sca=1 pc_sca=1 gc_sca=1 rwf_sca=1 fwf_sca=1
X1 node31 inp GND DELAY_CKT tcy:1000e-12
X2 node29 inn GND DELAY_CKT tcy:1000e-12
    
```

Fitting for Accuracy

The screenshot displays the SIMDE V1.0 interface. The main window shows a circuit diagram with a subcircuit 'X1' (Model1.mdl) containing a multiplier 'X'. A voltage source 'V1' is connected to the input, and a resistor 'R1' (R=100ohm) is connected to the output. A differential voltage probe 'probe1' is connected across the resistor. The 'Fitting' tab is active, showing a table of fitting results.

Fitting Report - Model: Model1

| ID | Probe | DAI(%) | DPI(%) | DA | DP | \$pu1 | \$pu2 |
|----|--------|--------|--------|------|------|-------|-------|
| 0 | probe1 | 9.34 | 34.75 | 0.05 | 0.19 | 0.6 | 0.95 |
| 1 | probe1 | 9.47 | 42.28 | 0.05 | 0.23 | 1.5 | 0.95 |
| 2 | probe1 | 5.42 | 38.15 | 0.03 | 0.21 | 0.96 | 0.95 |
| 3 | probe1 | 6.74 | 36.82 | 0.04 | 0.20 | 816m | 0.95 |
| 4 | probe1 | 5.90 | 37.54 | 0.03 | 0.20 | 902m | 0.95 |
| 5 | probe1 | 5.61 | 37.91 | 0.03 | 0.20 | 937m | 0.95 |
| 6 | probe1 | 5.47 | 38.05 | 0.03 | 0.20 | 951m | 0.95 |
| 7 | probe1 | 12.70 | 34.98 | 0.07 | 0.19 | 0.96 | 0.4 |
| 8 | probe1 | 9.38 | 40.30 | 0.05 | 0.22 | 0.96 | 1.5 |
| 9 | probe1 | 5.20 | 38.54 | 0.03 | 0.21 | 0.96 | 1.06 |
| 10 | probe1 | 6.98 | 39.37 | 0.04 | 0.21 | 0.96 | 1.24 |
| 11 | probe1 | 5.92 | 38.78 | 0.03 | 0.21 | 0.96 | 1.13 |
| 12 | probe1 | 5.55 | 38.64 | 0.03 | 0.21 | 0.96 | 1.09 |
| 13 | probe1 | 5.29 | 38.58 | 0.03 | 0.21 | 0.96 | 1.07 |

Parameter editor

| Name | Value | Start | Stop | Step |
|-------|-------|-------|------|------|
| \$pu1 | 0.6 | 0.6 | 1.5 | |
| \$pu2 | 0.4 | 0.4 | 1.5 | |

Structure

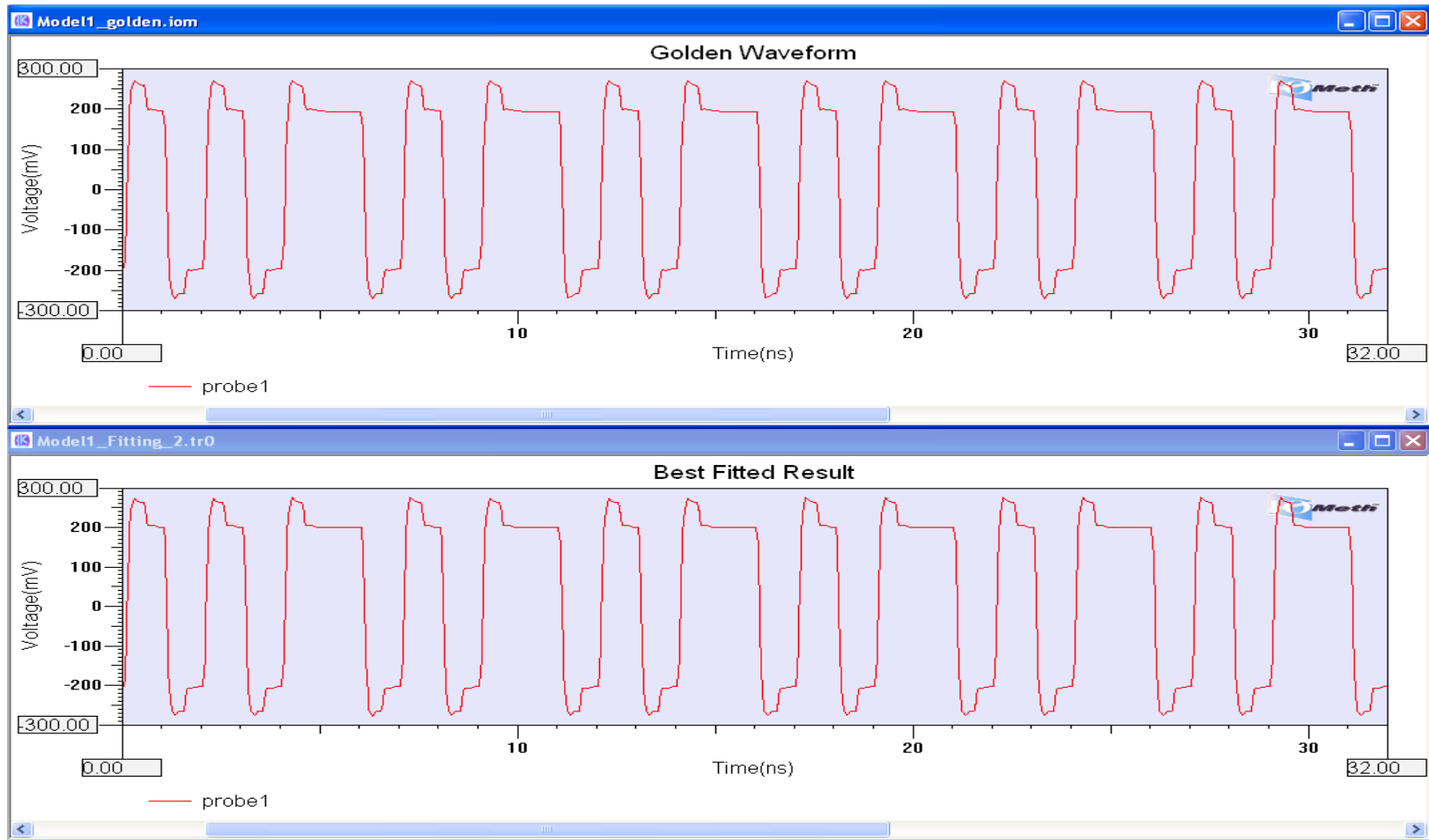
```

X1 node1 node2 node7 node8 Model1 pu1=pu1 pu2=pu2
R1 node7 node8 R=100
V1.+ node1 GND CUSTOMISED
V1.- node2 GND CUSTOMISED
    
```

Preference

- Typical
- Fast
- Slow

Fitting Result (DPI:1.14%, DAI:1.49%)

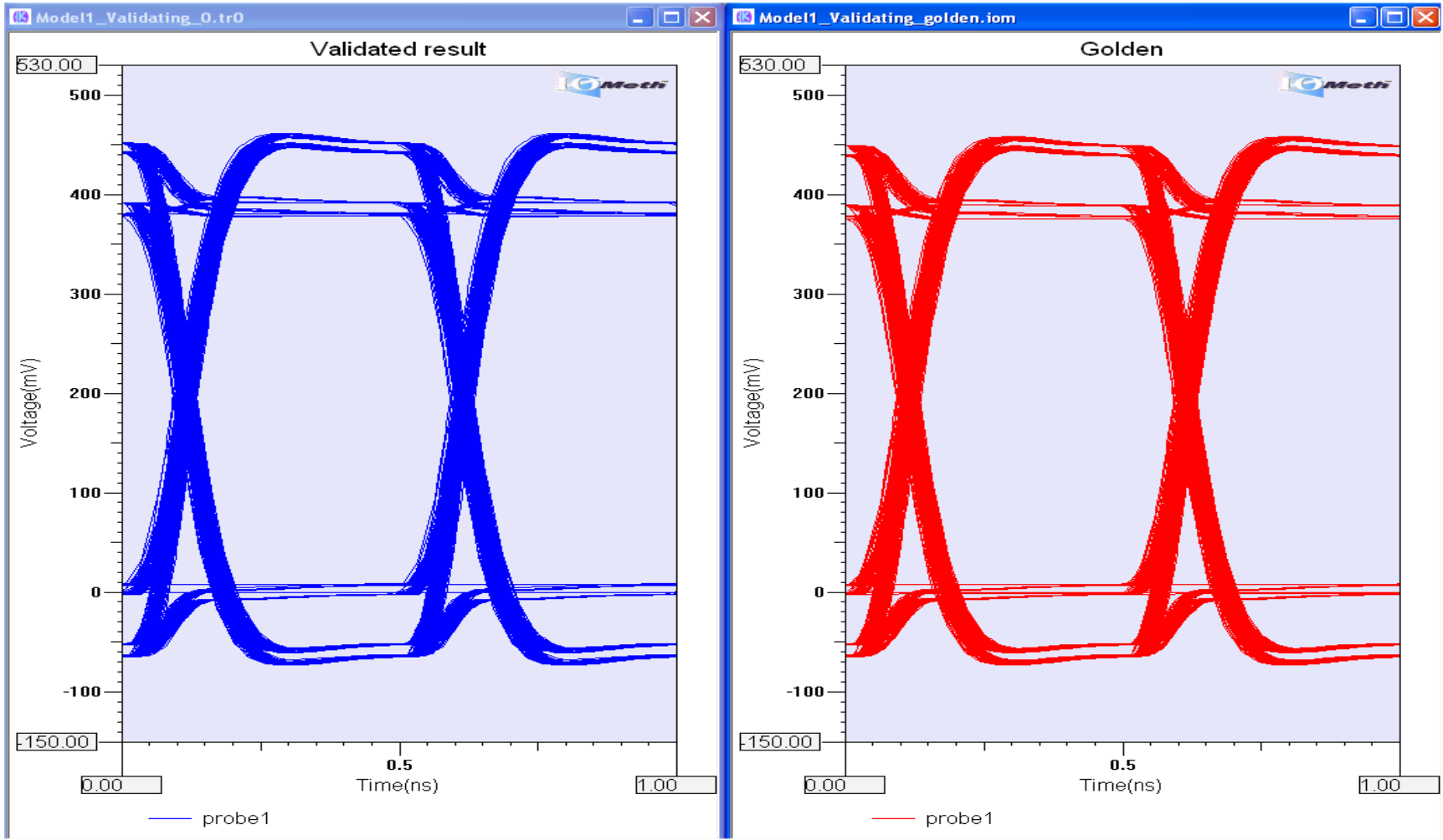


Free-Form Topology Editor for Validation

The screenshot displays the SIMDE V1.0 software interface. The main workspace shows a circuit diagram on a grid. The circuit includes a voltage source V1 connected to a subcircuit X1 (Model1.mdl). The subcircuit X1 has two input ports (inp, inn) and two output ports (outp, outn). The circuit is composed of several components: two transmission lines (T2, T3) with Z0 = 55ohm and L = 3ns; two capacitors (C1, C2) with C = 15uF; two transmission lines (T1, T4) with Z0 = 50ohm and L = 1ns; and a resistor (R1) with R = 100ohm. A differential voltage probe labeled 'probe1' is connected across the output ports. The bottom panel shows a netlist for the circuit:

```
X1 node1 node2 node8 node11 Model1 pd1=pd1 pu1=pu1
V1.+ node1 GND
V1.- node2 GND
R1 node16 node7 R=100
T1 node5 GND node16 GND TD=7.09n Z0=50 L=141m
T2 node8 GND node19 GND TD=7.09n Z0=55 L=423m
T3 node11 GND node21 GND TD=7.09n Z0=55 L=423m
T4 node13 GND node7 GND TD=7.09n Z0=50 L=141m
C1 node19 node5 C=15u
C2 node21 node13 C=15u
```

Validation Result



The Modeling Specialist

IO ***Meth***TM

<http://www.iometh.com>